

REMARKS

No claims have been cancelled and no new claims have been added by this response. Thus, claims 1, 2, 4-33, 35-44, 46, 48, 54, 56, 92-95 are pending in this application. For at least the following reasons, it is respectfully submitted that this application is in condition for allowance.

In the Action, Claims 1, 2, 6-28, 32-33, 37-42, 46, 48, 50, 52, 54, 56, 94 and 95 are rejected under 35 U.S.C. 102 (b) as being anticipated by Miyajima. Initially, it is noted that claims 50 and 52 had been cancelled by Amendment filed November 28, 2006 so that no augment will be made to claim 50 and 52 in the following response. The invention defined in independent claims 1 and 32 relates to a sealing apparatus for sealing a semiconductor wafer having semiconductor elements on its surface by resin. The characteristic of the invention claimed in claims 1 and 32, and the differences between the invention defined in claims 1 and 32 and Miyajima are clearly explained in the Paper submitted on September 28, 2005 on page 18, lines 5-13 (characteristic) and lines 14-20(differences). Namely, the characteristic of the invention claimed in claims 1 and 32 is,

- (a) a lower mold having a first area where the semiconductor wafer is to be mounted, wherein the lower mold has an uneven surface, which is formed within a second area, which is in the first area, and wherein the uneven surface is not formed in the periphery of the first area.

It is clear from claims and from the above-described characteristic that the semiconductor wafer is not mounted in the second area. As described in the specification of the present invention on page 10 lines 8-15,

according to the structure described above, if the uneven surface exists under the periphery of the semiconductor wafer 201, large force may be focused on the periphery of the semiconductor wafer 201. As a result, the force in the range between a few tons and a few decades of tons is applied to the sealing device 100.

As to the differences from Miyajima, Miyajima does not disclose this characteristic at all. As explained in Paper filed November 28, 2006, the device disclosed in Miyajima in Fig. 17 includes a lower die 20 having an area enclosed by sucking holes 76a. The surface in the area is mat-finished to form fine projections. As shown in Fig. 17, it is clear that the area enclosed by the sucking holes 76a is much larger than an area where a semiconductor wafer is placed. It is also clear from Fig. 16 of Miyajima, uneven surface is formed in the entire area enclosed by the sucking holes 96, which correspond to the first and second areas of the present invention. Thus, the fine projections are arranged under the peripheral area of semiconductor wafer when the semiconductor wafer is sandwiched between the upper and lower dies. Applicant understands that Miyajima discloses the device having fine projections at the bottom of the cavity. However, the fine projections are formed on the entire surface of the cavity in order to position a release film accurately in Miyajima. Please refer the column [0059] of Miyajima. In addition, in Fig. 16 of Miyajima, the entire surface of the circular contacting-by-pressing side 20c, which contacts by pressing the semiconductor wafer 90 and its periphery that is the entire area encompassed by the air adsorption holes 96, are formed with fine projections, and it is also clear from Fig. 17 that the fine projections are formed on the entire surface of the area which is encompassed by the air adsorption holes 76a. Therefore, Miyajima is quite

different from the invention at the point that the uneven surface is not formed in the periphery of the first area.

In view of the rejection to claim 6 and the examiner's assertion in Response to Arguments dated February 27, 2007, the examiner understands that the second area corresponds to the surface of the clamper 76 of Miyajima. **This is clearly wrong.** It is clear from Fig. 15 of Miyajima that the semiconductor wafer 90 is not mounted on the clamper 76. In other words, the surface of the clamper 76 of Miyajima does not even include a first area of the invention where the semiconductor wafer is mounted. Thus, no advantage described above can not be obtained from the disclosure of Miyajima.

Further, the examiner asserts that the slits 96, 98, 76a and 77 of Miyajima form uneven surface within a second area. **This is also clearly wrong.** The location of the slits 96, 98, 76a and 77 does not located within the second area. First, according to the disclosure of the invention, an element with the reference number 76a is air adsorption hole, an element with the reference number 77 is adsorption groove, an element with the reference number 98 is cavity, and an element with the reference number 98a is an air vent hole. It is understood that forming these elements is interpreted as a formation of the uneven surface by the examiner. However, the limitation in claim 6 or claim 10 is that an area within slits as shown in Fig. 3 or within a single spiral slit as shown in Fig. 4 is formed with uneven surface. Thus, it is respectively pointed out that the examiner misunderstands the disclosure of the Miyajima.

Therefore, since Miyajima does not disclose or suggest the claimed sealing apparatus having the characteristic (a) described above, claims 1 and 32 clearly are not anticipated by Miyajima, and is deemed to be clearly patentable over Miyajima, and the rejection of claims 1 and 32 accordingly should be withdrawn.

Further, claims 2, 6-28, 33 and 37-42 depend from claim 1 or claim 32 directly or indirectly. Since Applicants believes that claims 1 and 32 includes a patentable subject matter, the rejection of claims 2, 6-28, 33 and 37-42 depended from claim 1 or claim 32 should be withdrawn.

As to Claim 46, 48, 54, 56, 94 and 95, the characteristic of the invention claimed in independent claim 46 is,

(b) shock absorbers buffering stress to the semiconductor wafer, wherein a **part of each shock absorber is exposed in an area where the semiconductor wafer is to be mounted**, and wherein the shock absorbers are disposed symmetrically against the center of the area.

As described in the specification on page 11 lines 9-18, according to the structure described above, in addition to buffering stress applied to the semiconductor wafer, the shock absorbers serve to adapt to the varieties of the thickness of each of the semiconductor wafers because they are located in the area where the semiconductor wafer is to be mounted, and because the plurality of shock absorbers are disposed in a balanced manner. As a result, the resin having uniform thickness can be formed even if the semiconductor wafers having a different thickness are set in the sealing apparatus defined in claim 46.

As described in Paper filed November 28, 3006, however, Miyajima does not disclose this characteristic at all. As the examiner suggested, the shock absorbers 78 are disclosed in Figs. 13-15. However, none of the shock absorbers 78 is exposed in the area where the semiconductor wafer is to be mounted. It is clear from Fig. 14 that the shock absorbers 78 are disposed outside an area where the semiconductor wafer is to be mounted. Thus, it may be difficult for Miyajima's device to adapt to the varieties of the thickness of each of the semiconductor wafers.

In addition, in Fig. 16 of Miyajima, although it seems that the shock absorber 78 is disposed in a location facing to a good-to-be-mold 16, it should be noted that the good-to-be-mold 16 is not a semiconductor wafer. This is clear from Fig. 14 that it shows the example of the resin sealed semiconductor wafer. Further, a good-to-be-mold 16 is mounted on the upper mold, not on the lower mold so that Miyajima has no idea that each shock absorber is exposed in the area where the semiconductor wafer is to be mounted, and that the shock absorbers are disposed symmetrically against the center of the area.

As to the above-described argument, the examiner asserted on page 9, lines 2-6 that Miyajima teaches a part of each shock absorber 78 is exposed in the area where the semiconductor wafer is to be mounted, and by referring Fig. 14, the area is located between a base block 74 and an upper part of the shock absorber 78, and the area is also located between the shock absorber 78 and an area under lower mold 21. The exposed area is labeled with a downward arrow. This is clearly wrong. The shock absorber 78 of Miyajima is located outside the first area where the semiconductor wafer 90 is mounted. This incorrect

interpretation by the examiner is caused in that the examiner understands that the surface area of the clasper 76 is considered as the second area. **Please consider the second area of the invention is located within the first area, not outside the first area.**

Therefore, since Miyajima does not disclose or suggest the claimed sealing apparatus having the characteristic (b) described above, claim 46 clearly is not anticipated by Miyajima, and is deemed to be clearly patentable over Miyajima, and the rejection of claim 46 accordingly should be withdrawn.

Further, claims 48, 54, 56, 94 and 95 depend from claim 46 directly or indirectly. Since Applicants believes that claim 46 includes a patentable subject matter, the rejection of claims 48, 54 and 56 depended from claim 46 should be withdrawn, and new claims 94 and 95 should be allowed.

In the Action, claims 4, 5 and 36 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Miyajima. Initially, claims 5 and 36 depends from claims 1 and 32, respectively. Applicants believes that claims 1 and 32 include a patentable subject matter, the rejection of claims 5 and 36 depended from claims 1 and 32 should be withdrawn. Claim 4 is also rejected under 35 U.S.C. 103(a) over the Miyajima and Tago. Thus, the argument against Miyajima will be made together with the argument against Miyajima and Tago below.

In the Action, Claims 29-31 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Miyajima in view of Yamamoto. Claims 29-31 are dependent claims, each of which depends from Claim 1 indirectly. Thus, these claims include

all limitation of Claim1. As described above, Miyamoto does not disclose the characteristic (a) described above.

As to Yamamoto, it simply discloses a mold device for resin sealing. However, Yamamoto does not disclose a characteristic (a) described above at all. In addition, Yamamoto discloses the mold for sealing an individual semiconductor chip, not wafer, in the condition that the chip is mounted on a lead frame. This is a huge difference from the invention for sealing a semiconductor wafer because there are no problems for the individual chip to be cracked in the sealing process so that no improvement in the uneven surface field is necessary.

As to the arguments for the impossibility of the combination of the references, which have been made in Paper filed November 28, 2006, Applicant drops the reasons (no common nature of problems between references), which is the basis of the argument, to the current claims in view of *KSR International v. Teleflex Inc.*, U.S. Supreme Court No. 04-1350 (April 30, 2007). However, Applicant maintains his position that Miyajima and Yamamoto cannot be combined because of the reasons below. According to *KSR Int. id*, the findings in *Graham v. John Deere Co.*, of Kansas City, 383 U.S. 1 (1966) is not changed. Rather, the problem is that the Federal circuit addressed the obviousness question in a narrow, rigid manner that is inconsistent with 103. Thus, it is still required to show the STM (suggestion-Teaching-Motivation). According to the *KSR Int.* U.S. Supreme Court No. 04-1350 (April 30, 2007), more important approach is that any need or problem known in the field and addressed by the patent can provide a reason for combining the elements in the manner claimed. Applicants understand that Yamamoto discloses the individual semiconductor chip, which has already been

divided from the semiconductor wafer, and Miyajima discloses that the release film is placed between the mold and semiconductor wafer. This means that there are no common or overlapped problems to all of them. Thus, in view of the disclosure of Yamamoto, Miyajima and the invention, it should be concluded that no need or no problem known in the field and addressed by the patent exists to provide a reason for combining the elements in the manner claimed.

Accordingly, neither Miyajima nor Yamamoto suggest or disclose the characteristic described above, claims 29-31 clearly are not obvious over Miyajima in view of Yamamoto, and is deemed to be clearly patentable over them, and the rejection of claims 29-31 accordingly should be withdrawn.

In the Action, Claims 4, 35, 92 and 93 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Miyajima in combination with Tago. The characteristic of the invention claimed in claims 4 and 35 includes that the uneven surface has a roughness in a range between 8 μ m and 12 μ m. According to this structural characteristic, it is possible to avoid making any damage to a semiconductor wafer, and to avoid adhering a semiconductor wafer to the mold.

However, as described in Paper filed November 28, 2006, Miyajima does not disclose or suggest any size of the fine projection. As examiner also well pointed out, Miyajima fails to teach forming a wafer or substrate directly on the surface of mold or lower mold. However, the examiner asserts that it would be obvious to one of the ordinary skill in the art of making semiconductor device to determine the workable or optimal value or range for the surface roughness through routine experimentation and optimization to obtain optimal to desired

device performance. **Applicant disagrees.** In Miyajima, a release film 41 is placed between the semiconductor wafer and the cavity so that the semiconductor wafer may not be directly contact with the lower mold. Thus, even if the uneven surface formed in the second area is disclosed in Miyajima (actually not disclosed, but "if"), the unevenness would be absorbed by the release film. Under this structural differences, Applicant has no idea why the range of the roughness of the uneven surface would be obvious to one of the ordinary skill in the art. Namely, Miyajima has no idea to avoid making a scratch on the semiconductor wafer by considering the size of the fine projection. On the other hand, the semiconductor wafer directly placed on the rough surface in the present invention, and when the uneven surface is set in a roughness in a range between $8\mu\text{m}$ and $12\mu\text{m}$, it would be possible to avoid making scratches on the semiconductor surface.

As to the combination with Tago, as well as Yamamoto, Miyajima and Tago cannot be combined because of the reason below. The examiner asserts on page 9, lines 12-14 that Tago teaches a molding apparatus in which the substrate 57 is mounted directly on a surface of the lower mold 60 to prevent reduction in yield. However, Tago discloses for sealing the substrate 57 on which an individual semiconductor chip, which is dived from the semiconductor wafer already, is mounted. Thus, as explained and introduced above as to the issue of the combination matter, since **no need** or **no problem** known in the field and addressed by the patent exists to provide a reason for combining the elements in the manner claimed, these references cannot be combined.

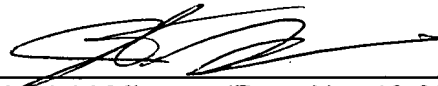
Accordingly, neither Miyajima nor Tago suggest or disclose that the uneven surface has a roughness in a range between $8\mu\text{m}$ and $12\mu\text{m}$, claims 4 and 35

clearly are not obvious over Miyajima and Yamamoto, and is deemed to be clearly patentable over them. Claims 92 and 93 depend from claims 4 and 35, respectively so that claims 92 and 93 should also be patentable.

Claims 43 and 44 are allowed.

In view of the foregoing, the application is deemed to be in condition for allowance and such is earnestly solicited. Should any fee be needed, please charge it to our Account No. 50-0945 and notify us accordingly.

Respectfully submitted,



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